What is claimed is:

1	1.	An electronic structure comprising:	
2	a firs	st dielectric layer of polymeric material having a first top surface;	
3	a sec	cond dielectric layer of polymeric material on said first top surface of said first	
4	dielectric lay	ver of polymeric material, having a second top surface, said second layer of	
5		naterial also having trench features therein; and electrically conductive material	
6	deposited in said trench features forming electrically conductive circuit lines being		
7	substantially flush with said second top surface of said second dielectric layer of polymeric		
8	dielectric material.		
1	2.	The electronic structure of claim 1 further including a third dielectric layer of	
2	dielectric po	lymeric material located on said conductive circuit lines.	
1	3.	The electronic structure of claim 1 wherein said electrically conductive	
2	material is plated metal.		
1	4.	The electronic structure of claim 3 wherein said plated metal is copper.	
1	5.	The electronic structure of claim 1 wherein said first dielectric layer of	
2	polymeric material is a different material than said second dielectric layer of polymeric		
3	material.		
1	6.	The electronic structure of claim 5 wherein said second dielectric layer of	
2	polymeric m	aterial is a polymer resin.	
1	7.	The electronic structure of claim 1 wherein the circuit lines are about 0.5 to	
2	about 1 mil v	vide, about 0.5 to about 2 mils apart and up to about 20 microns thick.	
1	8.	The electronic structure of claim 1 wherein the circuit lines are about 5 to	

about 20 microns thick.

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1	9.	The electronic structure of claim 1 wherein the circuit lines are 5 to about 10	
2	microns thick.		
1	10.	An electronic structure which comprises at least two of the structures of	
2	claim 1 stacke	d together.	
1	11.	A method of fabricating an electronic structure having embedded	
2	substantially fl	lush circuit features which comprises:	
3	providing a first dielectric layer of polymeric material with a top surface;		
4	deposi	ting a second dielectric layer of polymeric material on said top surface of	
5	said first layer	of polymeric material, said second dielectric layer of polymeric material	
6	also having a s	second top surface;	
7	definir	ng trench features with sidewalls and bottoms, in said second dielectric layer	
8	of polymeric material;		
9	provid	ing a seed layer only on said sidewalls and bottoms of said trench features;	
10	depositing electrically conductive material in said trench features such that said electrically		
11	conductive material is substantially coplanar with said top surface of said second dielectric		
12	layer of polyn	neric material.	
1	12.	The method of fabricating an electronic structure of claim 11 further	
2	including: dep	positing a third layer of dielectric polymeric material.	
1	13.	The method of claim 11 wherein said trench features are defined by laser	
2	ablating.	The medical of claim II wherein said deficit readules are defined by laser	
_	uotutiig.		
1	14.	The method of claim 13 wherein said seed layer is provided by blanket	
2	depositing a se	ed layer and then mechanically removing the seed layer from all non-laser	

trench features.

ablated surfaces thereby the seed layer remains only on said sidewalls and bottoms of said

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1	15.	The method of claim 11 wherein said seed layer is copper provided by	
2	depositing cor	per from copper acetyl acetonate gas by laser deposition thereby providing	
3		n said sidewalls and bottoms of said trench features.	
1	16.	The method of claim 11 wherein said conductive material comprises copper.	
1	17.	The method of claim 11 wherein said trench features are up to 20 microns	
2	thick.		
1	18.	The method of claim 11 wherein said trench features are about 5 to about 20	
2	microns thick.		
1	19.	The method of claim 11 wherein said trench features are about 5 to about 10	
2	microns thick.		
1	20.	The method of claim 11 wherein said seed layer comprises copper or	
2	chromium.		
1	21.	The method of claim 11 wherein the seed layer is about 100 angstroms to	
2	about 5000 ang		
1	22.	The structure obtained by the process of claim 11.	
1	23.	A method for fabricating a structure having embedded substantially flush	
2	circuitry features which comprises:		
3		providing a first layer of polymer resin having a metal dispersed therein and	
4	having a top surface;		
5	deposit	ing a second dielectric layer of a dielectric polymeric material on said top	
6	surface of said	first polymer resin, said second dielectric layer of a dielectric polymeric	

material also having a second top surface;

8	defining trench features with sidewalls and bottoms, in said second dielectric layer
9	of dielectric polymeric material and into said first layer of polymer resin and thereby
10	exposing metal in said sidewalls and bottoms of said trench features to provide a seed layer;
11	depositing electrically conductive material in said trench features such that the
12	electrically conductive material is substantially coplanar with said second top surface of said
13	second dielectric layer of a dielectric polymeric material.

- 1 24. The method of claim 23 wherein said conductive material comprises copper.
- 1 25. The method of claim 23 wherein said trench features are up to 20 microns 2 thick.
- 1 26. The method of claim 23 wherein said trench features are about 5 to about 20 2 microns thick.
- 1 27. The method of claim 24 wherein said trench features are about 5 to about 10 2 microns thick.
- 1 28. The method of claim 24 wherein said seed layer comprises copper or 2 chromium.
- 1 29. The method of claim 24 wherein said seed layer is about 100 angstroms to 2 about 5000 angstroms thick.
- 1 30. The structure obtained by the process of claim 23.
- 1 31. The method of claim 23 wherein said metal comprises copper powder.